URN etd-0407109-183705-306
Author Chen-Yang Tsai
Author's Email Address No Public.
Statistics This thesis had been viewed 57 times. Download 0 times.
Department
Year 2005
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Hardware/Software Co-design and Implementation of MPEG-4 Simple Profile Encoder on Xilinx Virtex2 Platform
Date of Defense 0000-00-00
Page Count 46

Keyword
MPEG-4
SOC
embedded system

Abstract
Because most of MPEG-4 encoders are implemented in software, the thesis implements the compression of MPEG-4 algorithms in the form of software/hardware co-design, named VCS (Video Coding System), and cooperates with x86 CPU. to form an SOC (System On a Chip). To make VCS cooperate with CPU, an software interface is designed to control data accessing between them. Besides, to reduce the number of operations of CPU and reach higher speed, all the access addresses will be calculated by the interface. Finally with practical operation of Xilinx Virtex2 FPGA, VCS uses nearly 1 million gates, and can operate at the speed of 36 MHz clock rate.
Advisory Committee - advisor

Files No Any Full Text File.
Date of Submission 2006-08-22